Claims

1. A feed forward equalizer for analog equalization of a data signal received over a data transmission channel comprising:

(a) a Master Delay Locked Loop (M-DLL) for generating equidistant reference phase signals;

(b) a Slave Delay Line (S-DLL) formed by serial connected Slave Delay Units (SDU),
wherein each Slave Delay Unit (SDU) has a Slave Delay Element (SDE) to delay the received data signal with a predetermined delay time (ΔT) and
an analog amplifier which amplifies the delayed output signal of the Slave Delay Element (SDE) with a respective weighting coefficient to generate a weighted delay signal,
wherein the analog amplifier is switched transparent in response to a corresponding reference phase signal generated by said Master Delay Locked Loop (M-DLL); and

(c) subtracting means for subtracting the weighted delay signals which are selected by means of a multiplexer from the received data signal to generate an equalized output data signal.

2. The feed forward equalizer according to claim 1, wherein the multiplexer is controlled by a control word stored in a control register.

3. The feed forward equalizer according to claim 1, wherein the weighting coefficients are stored in a coefficient register.

4. The feed forward equalizer according to claim 3, wherein the weighting coefficients are programmable by a control unit.

5. The feed forward equalizer according to claim 1, wherein the Slave Delay Line (SDL) comprises a predetermined number (N) of Slave Delay Units (SDU) which are connected in series.

6. The feed forward equalizer according to claim 1, wherein the Master Delay Locked Loop (M-DLL) comprises a predetermined number (N) of Master Delay Units (MDU) which are connected in series.

7. The feed forward equalizer according to claim 6, wherein each Master Delay Unit (MDU) includes a Master Delay Element (MDE) and an amplifier.

8. The feed forward equalizer according to claim 6, wherein the Master Delay Locked Loop (M-DLL) is clocked by a reference clock signal (CLK).

9. The feed forward equalizer according to claim 8, wherein the clock period (T_{CLK}) of the reference clock signal (CLK) is a fraction of the unit interval (UI) of the data signal.

10. The feed forward equalizer according to claims 1 to 9, wherein the Slave Delay Elements (SDE) are formed identical to the Master Delay Elements (MDE).

11. The feed forward equalizer according to claim 1, wherein all weighted delay signals are supplied to input terminals of the multiplexer which switches the weighted

delay signals through to a central summation point depending from a control word stored in said control register.

12. The feed forward equalizer according to claim 11, wherein the weighted delay signals which are switched through by said multiplexer are subtracted at the central summation point from the received data signal.

13. The feed forward equalizer according to claim 1, wherein each Slave Delay Unit (SDU) of the Slave Delay Line (SDL) further includes a decentral summation point to subtract the weighted delay signal form the received data signal.

14. The feed forward equalizer according to claim 13, wherein the decentral summation points of the Slave Delay Units (SDU) are connected to respective input terminals of the multiplexer which switches the decentral summation points through to an output of the multiplexer depending on the control word stored in said control register.

15. The feed forward equalizer according to claim 1, wherein the equalized output data signal is amplified by a post amplifier.

16. The feed forward equalizer according to claim 1, wherein the equalized output data signal is supplied to a decision unit.

17. The feed forward equalizer according to claim 1, wherein a buffer is provided for buffering the received data signal.

18. The feed forward equalizer according to claim 1,

wherein the data rate of the received data signal is more than 1 $\frac{Gbit}{sec}$.

19. Method for analog equalization of a received data signal comprising the following steps:

(a) generating equidistant reference phase signals by means of a Delay Locked Loop (DLL);

(b) delaying the received data signal by means of serial connected delay elements;

(c) amplifying the delayed output signals of the delay elements which respective weighting coefficients by means of analog amplifiers to generate weighted delay signals,
wherein the analog amplifiers are switched transparent in response to the reference phase signals generated by said Delay Locked Loop (DLL);

(d) selecting weighted delay signals by means of a multiplexer depending on a stored control word; and

(e) subtracting the selected weighted delay signals from the received data signal to generate an equalized output data signal.